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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROHISA MIYAZAWA

Appeal 2009-003845
Application 10/510,567
Technology Center 2800

Decided: August 31, 2009

Before JEFFREY T. SMITH, BEVERLY A. FRANKLIN, and LINDA M. GAUDETTE, *Administrative Patent Judges*.

SMITH, *Administrative Patent Judge*.

DECISION ON APPEAL

Statement of the Case

This is an appeal under 35 U.S.C. § 134 from a final rejection of claims 1, 3, and 5-10, all of the pending claims. We have jurisdiction under 35 U.S.C. § 6.[1]

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[1] In this decision we have considered Appellant's arguments presented in the Briefs, filed May 14, 2008 and September 24, 2008.

The claimed invention is directed to a circuit board device. Representative claim 1 is reproduced below.

1. A circuit board device for an information apparatus comprising:

a base board having mounted thereupon a plurality of low-frequency electronic components; and

a multilayer module board mounted at one surface of the base board and having mounted thereupon a plurality of high-frequency electronic components including at least a CPU and a memory, wherein:

the multilayer module board is one of

(i) a low-end module board,

(ii) a high-speed module board that operates at higher speed than the low-end module board or

(iii) an advanced function module board having more functions than the low-end module board; and

the base board is connected with one of

(i) the low-end module board,

(ii) the high-speed module board or
(iii) the advanced function module board.

Appellant appeals the Examiner's rejection of claims 1 and 5 as anticipated under 35 U.S.C. § 102(e) by Khosrowpour, U.S. Patent No. 6,477,593, issued November 5, 2002;

Claim 3 under 35 U.S.C. § 103(a) as obvious over the combination of Khosrowpour and Aruga U.S. Patent No. 6,085,137, issued July 4, 2000; and

Claims 6-10 under 35 U.S.C. § 103(a) as obvious over the combination of Khosrowpour and Yasuho U.S. Patent No. 5,346,402, issued September 13, 1994.

The issue before us is whether Appellant has shown that the Examiner reversibly erred in rejecting the claims under 35 U.S.C. §§ 102 (b) and 103(a). We answer this question in the affirmative. Therefore, WE REVERSE.[2]

The issue turns on whether Khosrowpour describes or suggests a multilayer module board mounted at one surface of the base board and having mounted thereupon a plurality of high-frequency electronic components including at least a CPU and a memory.

The Examiner bears the initial burden of establishing a prima facie case of anticipation. *In re King*, 801 F.2d 1324, 1326-27 (Fed. Cir. 1986). Anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *In re Robertson,* 169 F.3d 743, 745 (Fed. Cir. 1999).

The Examiner found that Figure 1 of Khosrowpour describes or suggests a multilayer module board (daughterboard 120) mounted at one surface of the base board and having mounted thereupon a plurality of high-frequency electronic components including at least a CPU (a bigger

[2] We select independent claim 1 as representative of the rejected subject matter.

chip, not labeled) and a memory (the three chips residing near the square chip (CPU)). (Ans. 3 and 7.)

Appellant contends that Khosrowpour does not disclose, expressly or inherently, a multilayer module board including at least a CPU and a memory. (App. Br. 8). We agree with the Appellant that the Examiner has not established that Khosrowpour necessarily includes a CPU and a memory on the multilayer daughterboard. The Examiner refers to the bigger, non-labeled chip of Figure 1. Throughout prosecution the Examiner has asserted that "the daughterboard typically, if not always includes a CPU and memory." (Ans. 7). To further support this position the Examiner has consistently cited another reference, not included in the statement of the rejection. (Ans. 7; Final Rejection, 6). In our opinion "typical if not always" is equivalent to a possibility or probability which is not the standard for establishing inherency for anticipation. *See In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981). As stated in *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (quoting from *In re Oelrich*, 666 F.2d at 581), "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency]" (emphasis in original). Under these circumstance, we cannot conclude that the Examiner has met the minimum threshold of establishing inherency under 35 U.S.C. § 102.

The Examiner's rejections of dependent claims 3 and 6-10 rely on the premise that Khosrowpour describes all the features of independent claim 1. More specifically, the Examiner has not relied upon the Aruga or Yasuho references for describing a CPU and a memory on a multilayer

daughterboard. Consequently, the rejections of claims 3 and 6-10 under 35 U.S.C. § 103 are reversed.

ORDER

The decision of the Examiner rejecting claims 1 and 5 under 35 U.S.C. § 102(e), and claims 3 and 6-8 under 35 U.S.C. § 103 (a) is reversed.

REVERSED

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